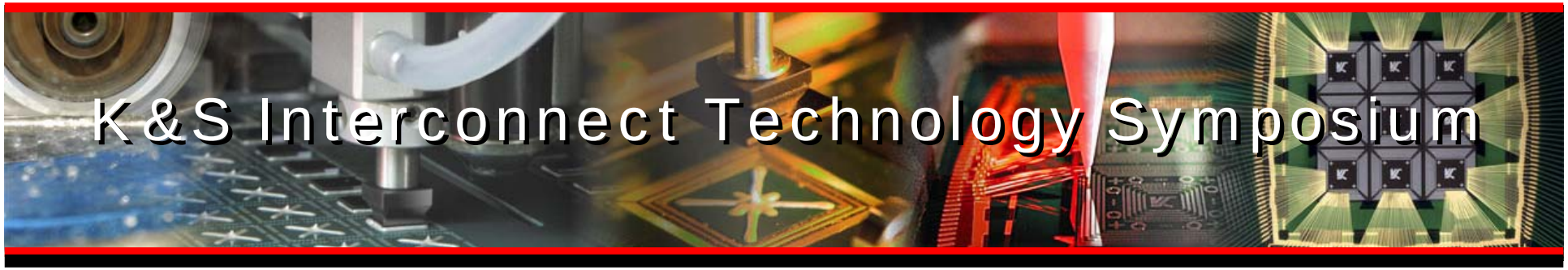
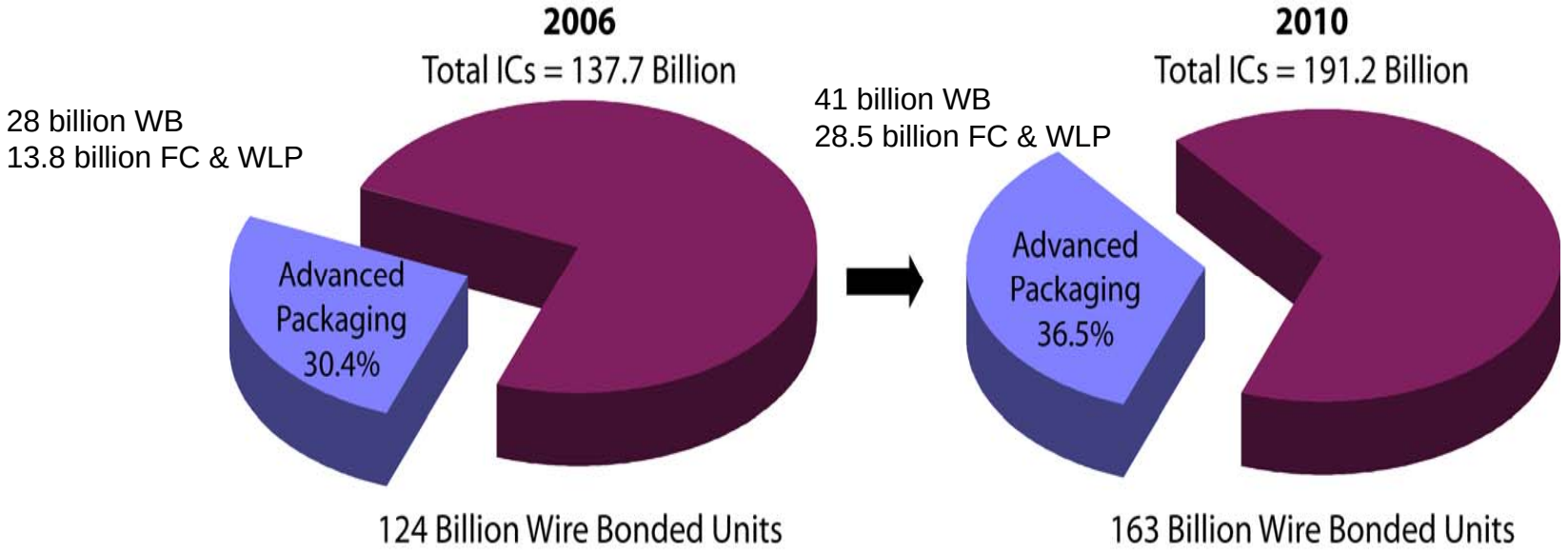


Advanced Packaging Interconnect Trends and Technology Developments

E. Jan Vardaman, President, TechSearch International, Inc.

Advanced Packaging Market Share



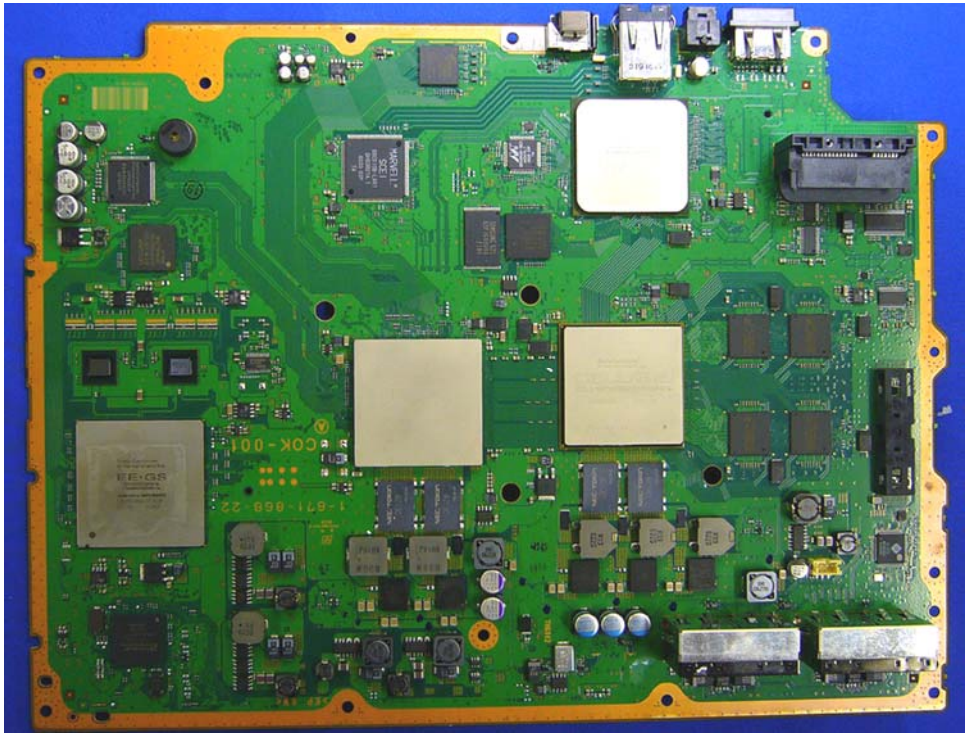
Source: IC Insights and TechSearch International, Inc.

- Advanced Packaging includes BGAs and CSPs, WLPs, and flip chip
- Growing in unit volume and dollar value

Drivers for Advanced Packaging Growth

- Mobile phones
  - More than one billion mobile phones expected to ship in 2007
  - Mobile phones contain an average 15 CSPs, including SiP
  - SiP for digital baseband section, transceiver section, RF section, camera module
  - Drives volumes for stacked die packages and system-in-package (SiP)
- Portable consumer products (digital camcorders, cameras)
  - Digital cameras/camcorders, MP3 players, DVD players, etc.
  - More than 100 million of Apple's iPods shipped since 2002
  - Thin is in…..drives new package technology developments
- Personal computers
  - PCs highest volume application for PBGAs
- Game machines
  - Growing volumes for PBGAs and CSPs

Sony's PS3 with BGAs and CSPs

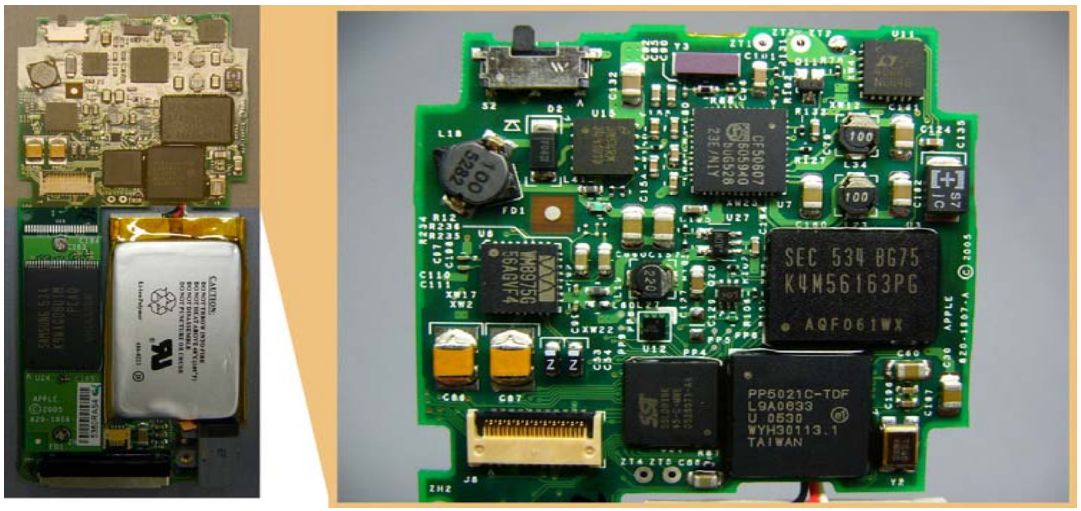


Source: http://pc.watch.impress.co.jp

- More than 20 BGAs and CSPs
- Leadframe parts including QFPs

Apple's iPod Nano

Source: Apple Inc.



Source: Adapted from Impress Corporation

- At least 7 CSPs on the main board, all wire bonded
- CSPs are underfilled
- 4 Gbit memory package in a TSOP, mounted on a daughter card
  2 Gbit memory mounted directly on the board

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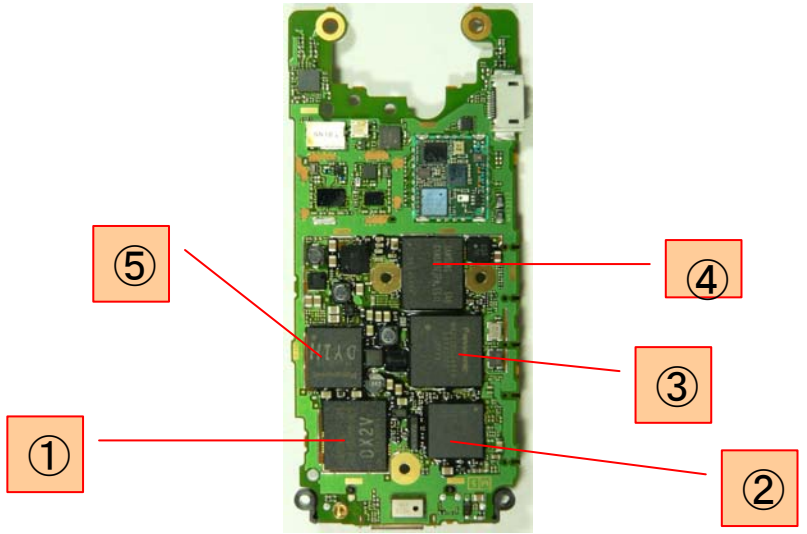
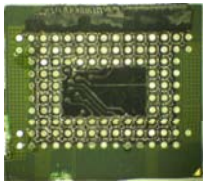
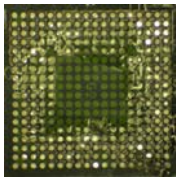
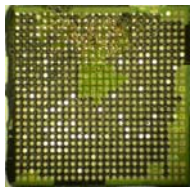
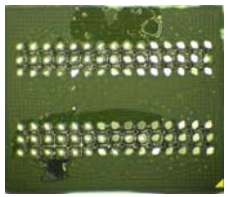
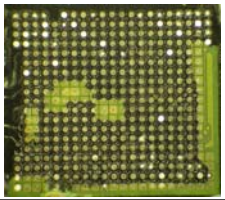
Panasonic P901iTV



Source: TPSS

	①	②	③	④	⑤
PKG TYPE	FBGA(L)	FBGA(L)	FBGA(L)	FBGA(L)	FBGA(L)
PIN COUNT	109	257	624	90	376
PKG SIZE (mm)	11.5x13.0	10.0x10.0	13.0x13.0	11.0x13.0	10.0x11.0
PKG Thickness (mm)	1.20	1.0	1.20	0.80	1.20
Terminal Pitch (mm)	0.80	0.50	0.50	0.80	0.50
					

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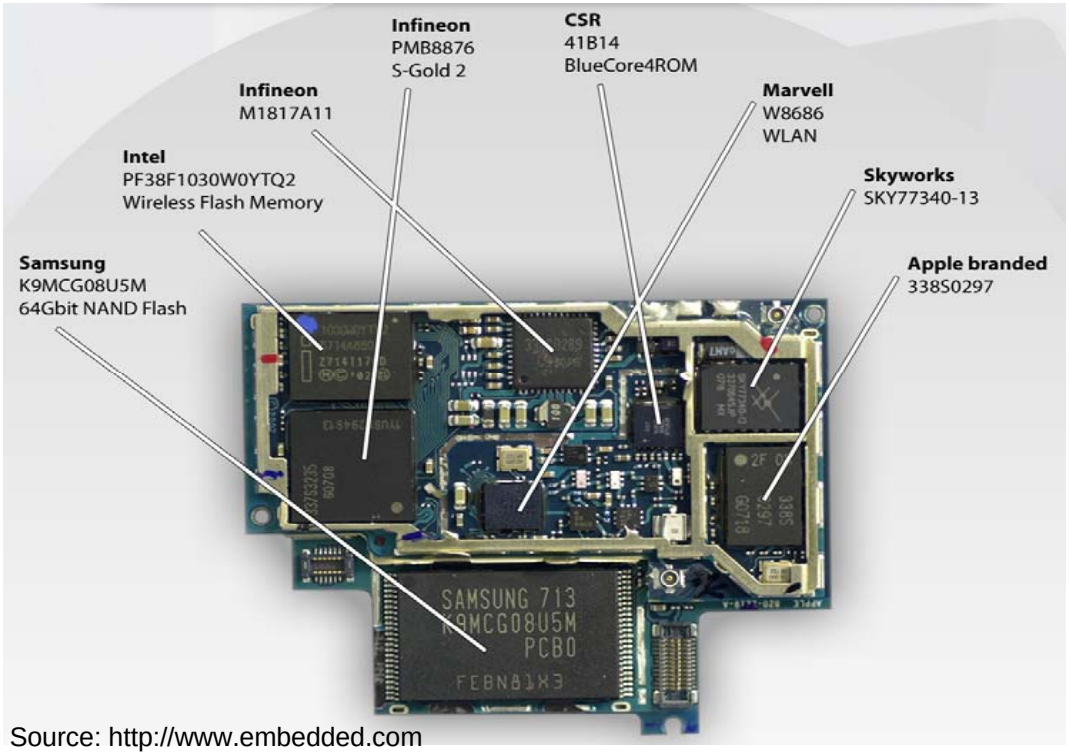
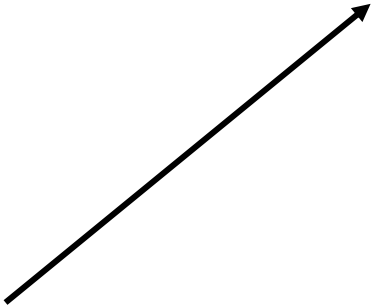
Apple's iPhone



Source: http://www.embedded.com

- More than 700,000 iPhones sold during the first weekend of product introduction
- Many wire bonded parts, a few WLPs

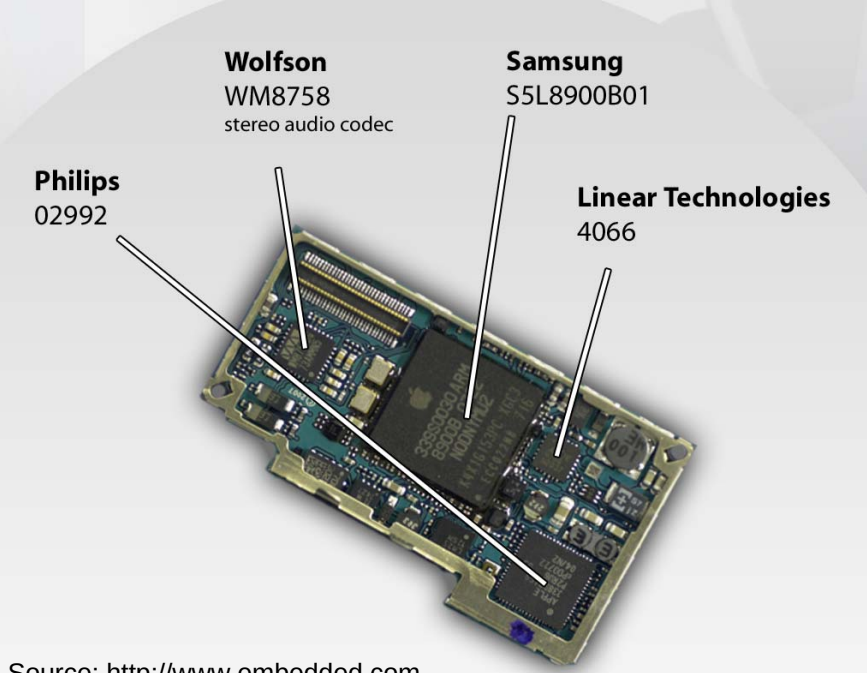
Apple's iPhone



QuickTime?and a
TIFF (LZW) decompressor
are needed to see this picture.

Intel stacked die package

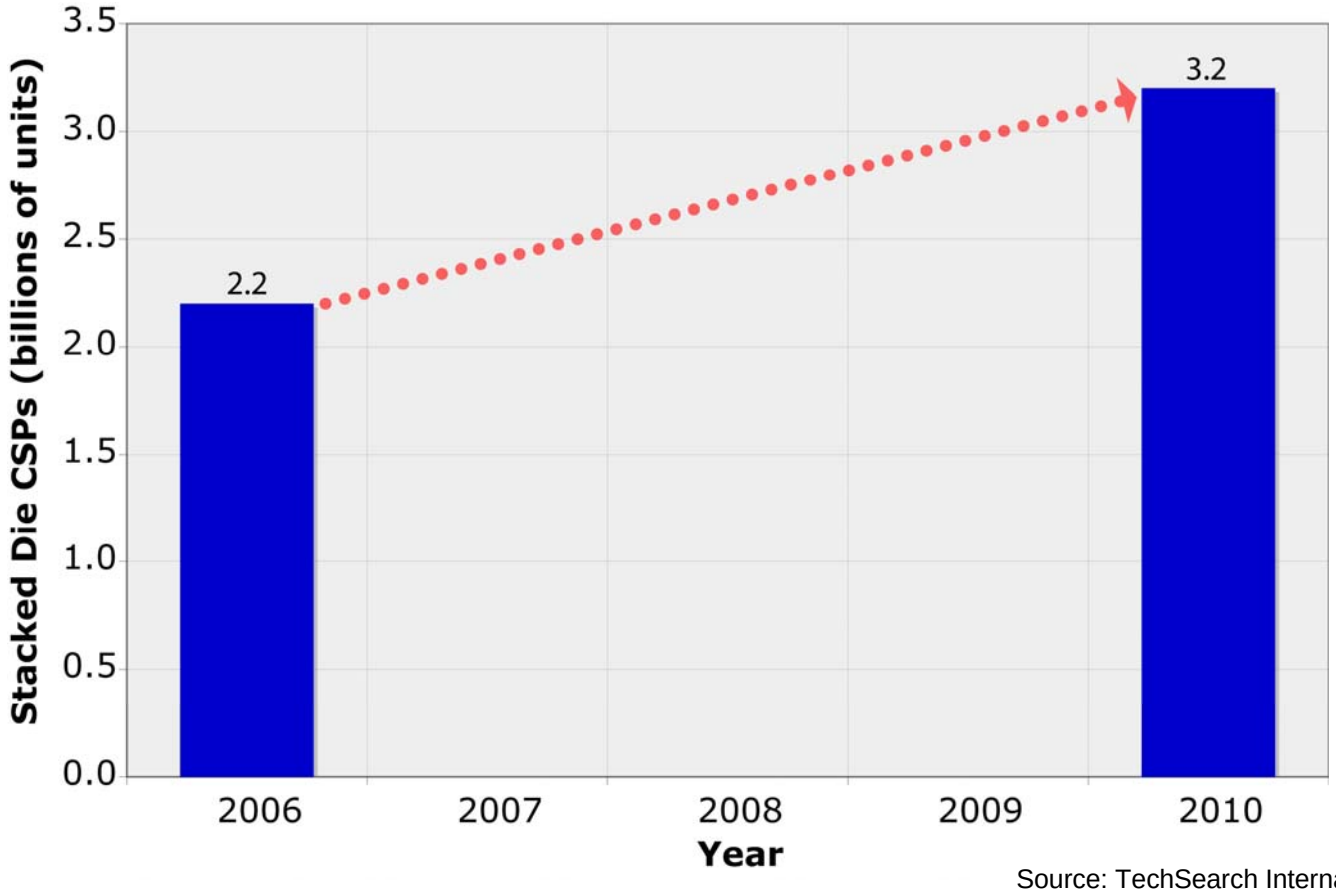
Apple's iPhone



Source: http://www.embedded.com

- Contains stacked die and PoP
- Samsung PoP with processor in the bottom package and two 512 Mbit SRAM die in the top stacked die package

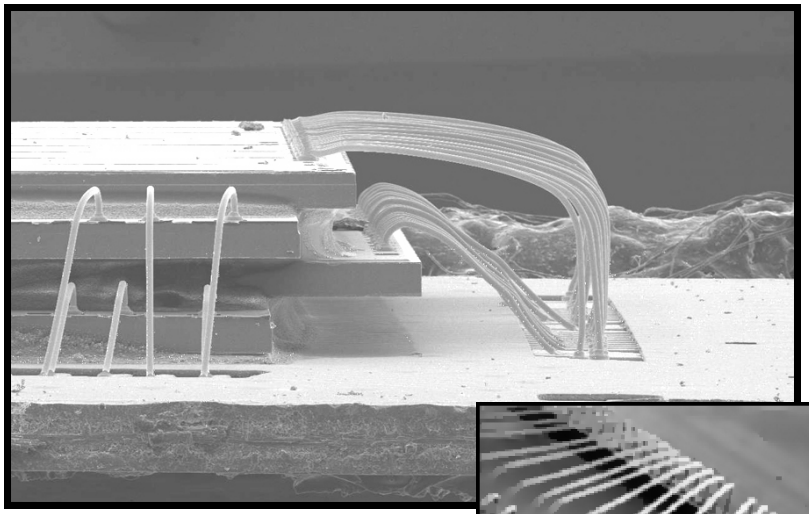
Stacked Die CSP Package Growth



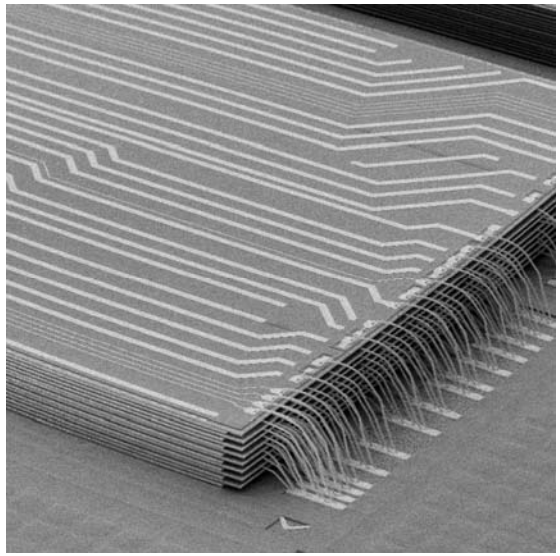
Source: TechSearch International, Inc

- Mobile phone is main growth driver
- Also found in digital cameras and camcorders
- CAGR 9.8%

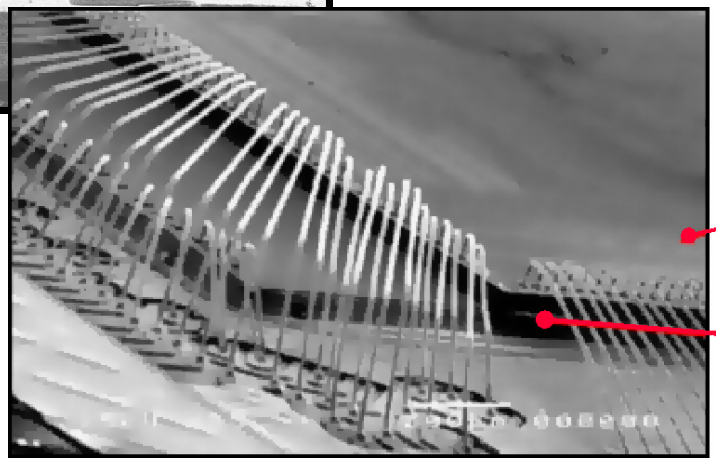
Stacked Die CSPs



Source: Intel



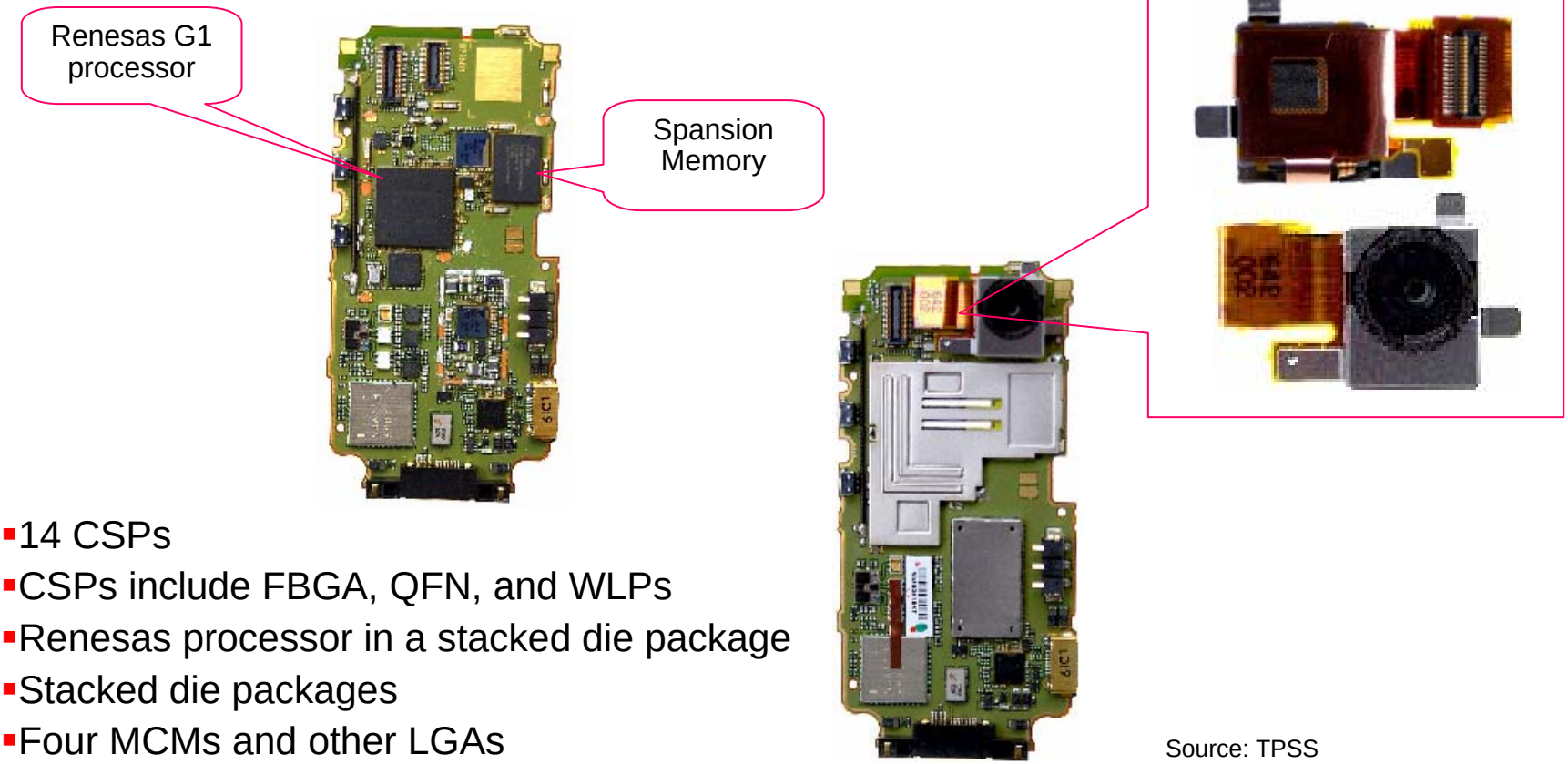
Source: Samsung



Source: TI

- 16 die stack demonstrated, 4-5 die per package common, typically 2 die per package in today's products
- Typically wire bond, but some gold stud bump (using ball bonder)

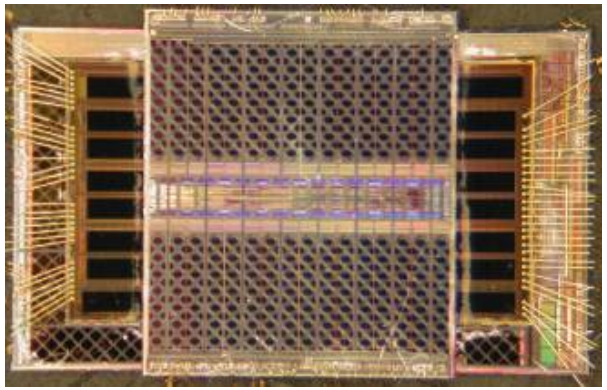
Fujitsu F903i Mobile Phone



- 14 CSPs
- CSPs include FBGA, QFN, and WLPs
- Renesas processor in a stacked die package
- Stacked die packages
- Four MCMs and other LGAs
- Packages typically wire bond
- CMOS image sensor camera module with 54 wire bonds

Source: TPSS

Spansion's Stacked Die in Fujitsu's F903i



Marking	98WS768P0GFA006
Body Size	9x13mm
Ball Pitch	0.80mm
Substrate THK	0.25mm
Mold Cap THK	0.79mm
PKG THK except Ball	1.04mm
Bonding Method	Wire Bonding
Die Configuration	2 Dies Stacked
Die size (Top die)	6.4x7.4x0.1mm
Die size (Middle die)	9.6x5.3x0.09mm
Die size (Bottom die)	11.7x6.9x0.09mm

Source: TPSS

- Two die stacked package
- Hundreds of wire bonds per CSP

Stacked Die in Fujitsu's F903i

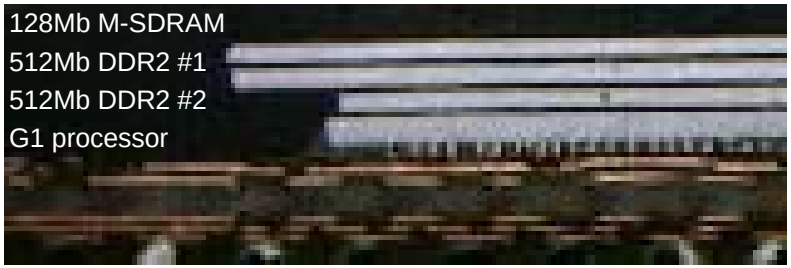
- SDRAM on top of 4 die stack
- Two DDR2 memory die mounted on Renesas G1 processor
- Total of 207 wire bonds in memory stack

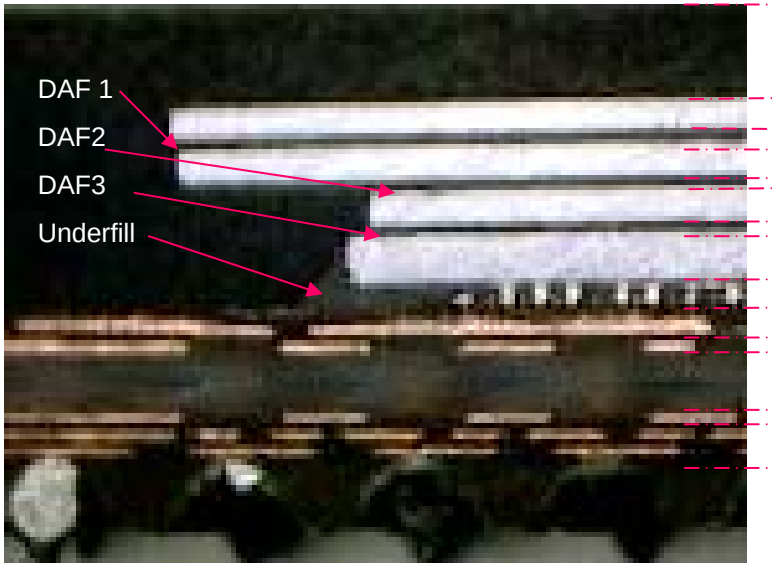
512Mb DDR2
BP size:
137x71um
BP pitch:
82um
Ball size:
37um ϕ
# of pads:
105 pads

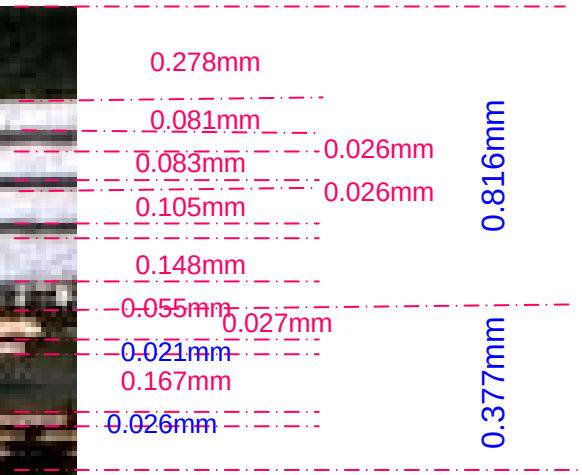
128Mb M-SDRAM
BP size:
137x57umum
82pitch:
81um
Ball size:
37um ϕ
# of pads:
102 pads

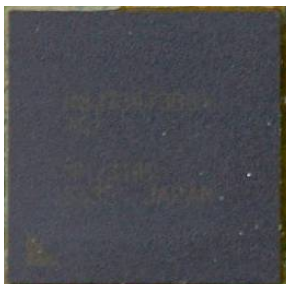
Source: TPSS

Stacked Die SiP in Fujitsu's F903i









Source: TPSS

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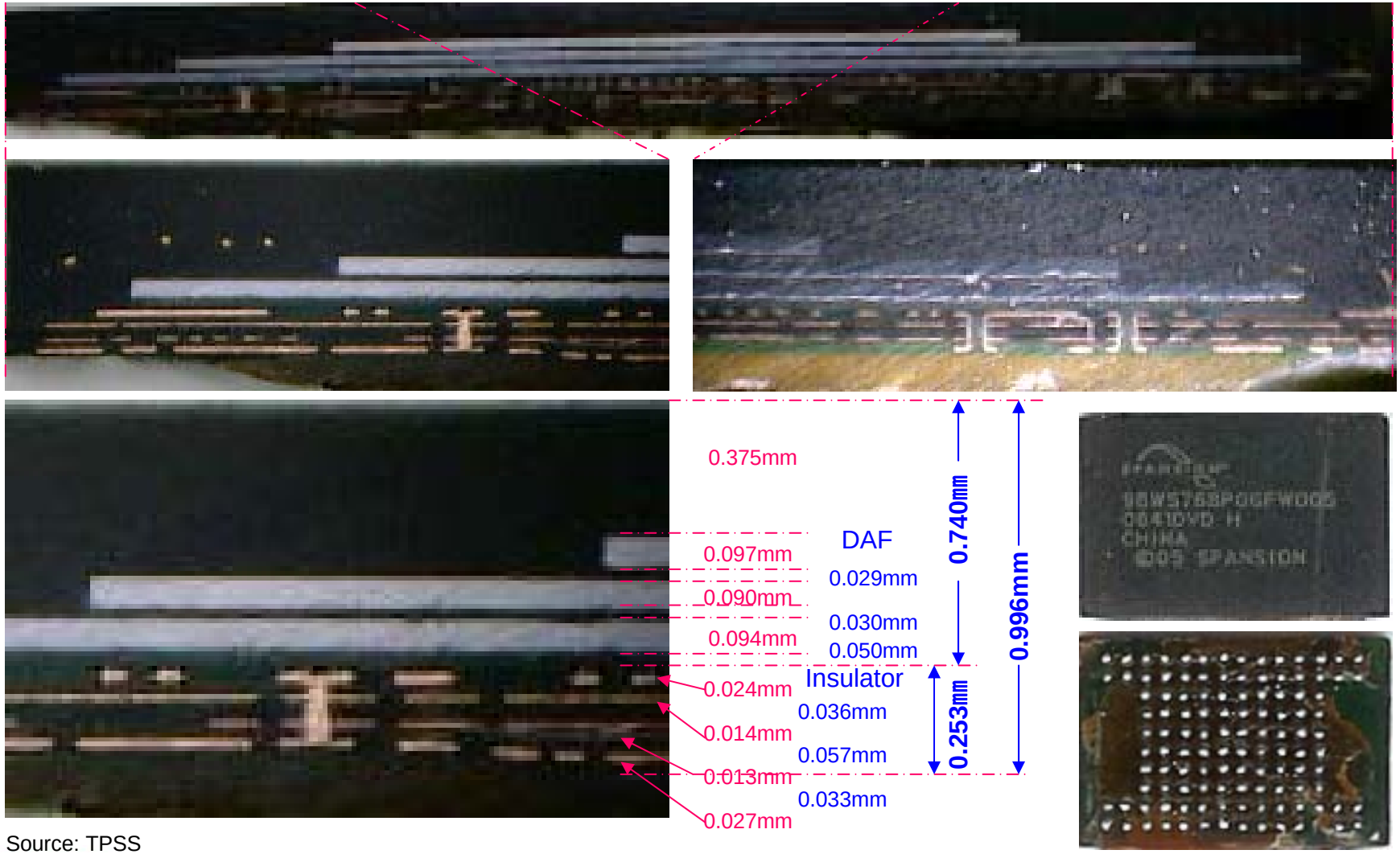
Spansion's Stacked Die in Fujitsu's F903i

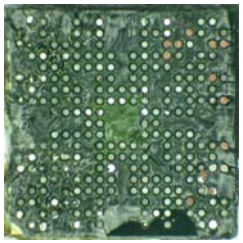


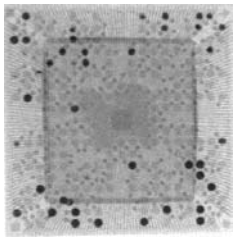
Source: TPSS

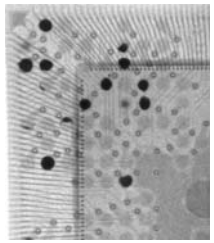
Kulicke & Soffa

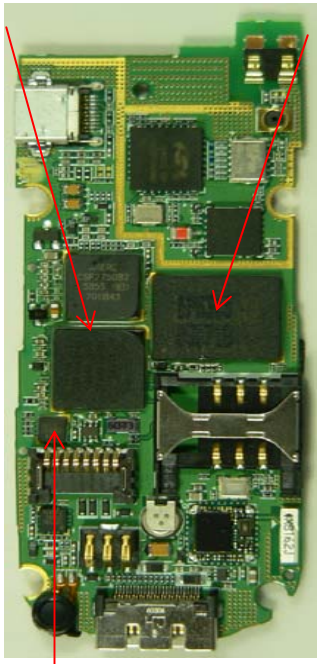
Samsung's X818 Phone with Stacked Die CSP

FBGA(L)224pin
10.0x10.0x1.20t
P=0.50
W/B 1chip

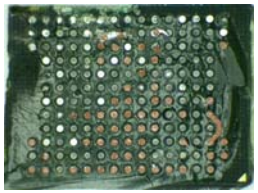


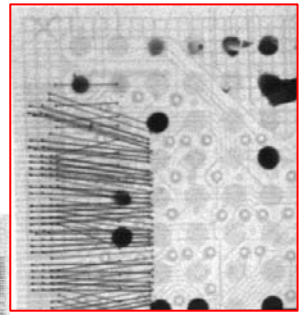


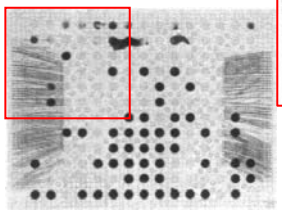


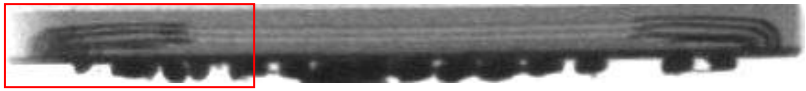


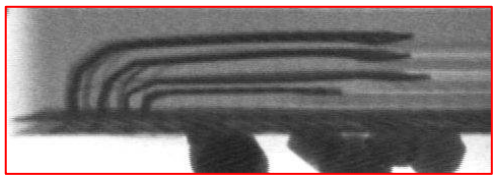
FBGA(L)
167pin
10.5x14.0x1.40t
P=0.80
W/B 4 chips



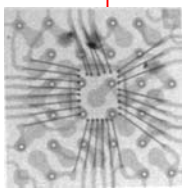








FBGA(L)
25pin
3.0x3.0x0.80t
P=0.50
W/B 1chip

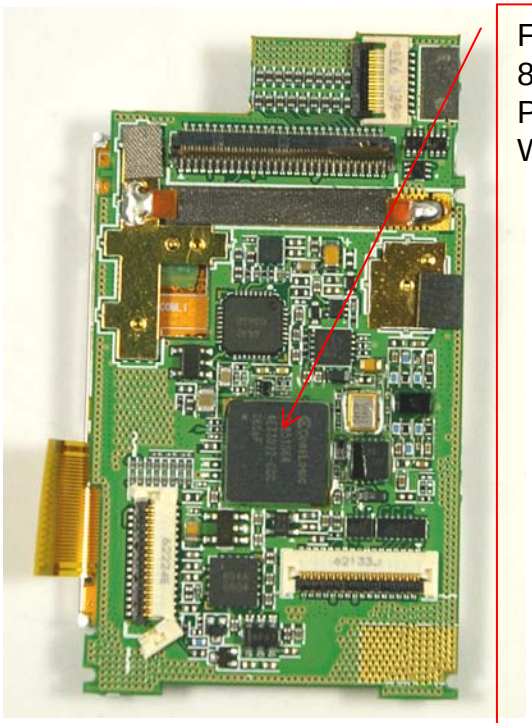


- Mobile phone for China market
  - Contains 18 CSPs plus several MCMs
  - Contains stacked die CSPs

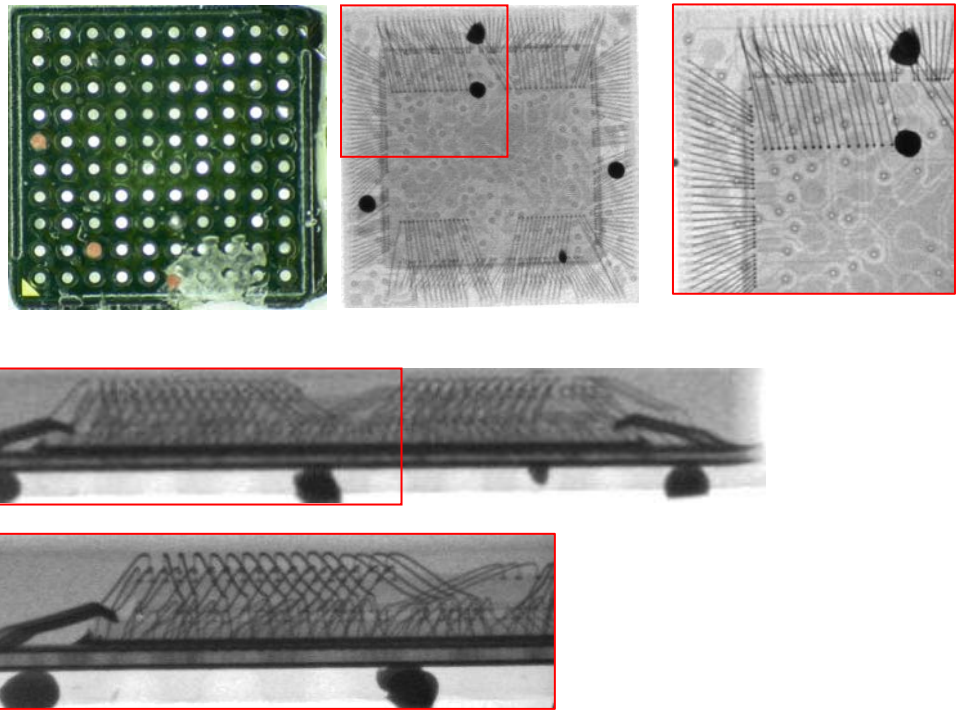
Source: TPSS

Kulicke & Soffa

Samsung's X818 Phone with Stacked Die CSP

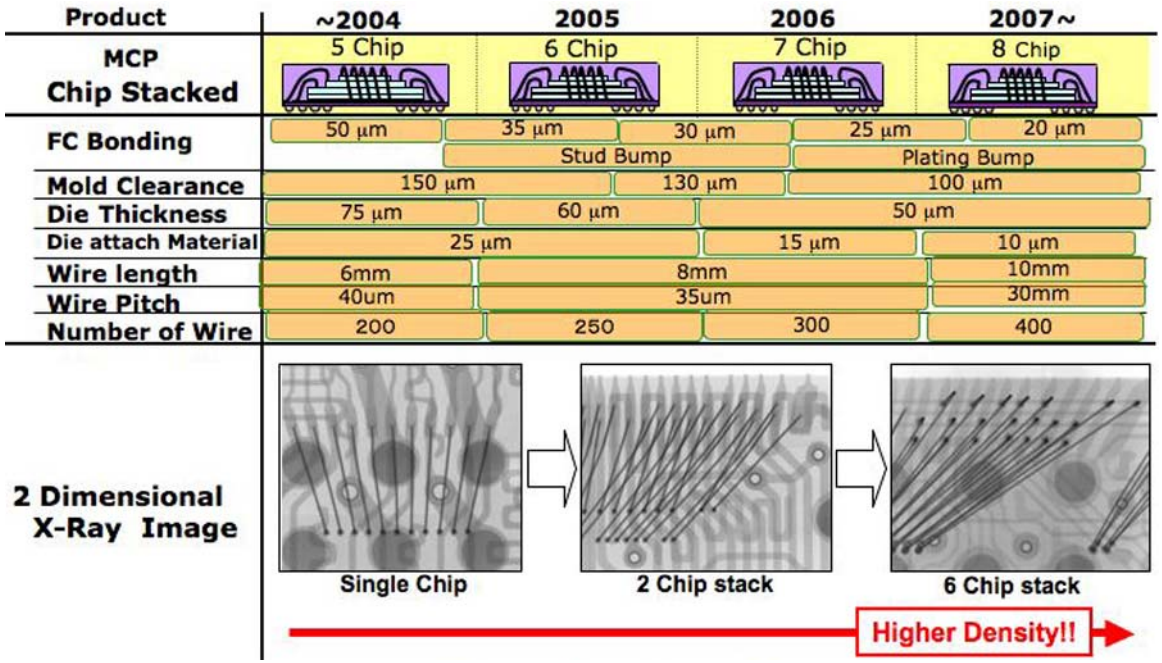


FBGA(L)100pin
8.0x8.0x1.20t
P=0.80
W/B 2 chips



Source: TPSS

Spansion's Roadmap for Die Stacking



Source: Spansion

- Number of die per stack has increased over time, and with it an increase in the number of wires
- Die thickness has decreased
- At the same time, pitch has decreased

Stacked Die Packaging Trends

- Thinner packages
  - From 1.2, 1.4 mm to below 1 mm.

→
- Thinner die
- Lower loop height
- Control of impact when bonding on overhang

- Higher level stacking
  - From 2, 3, 4 level to 5, 6, 7 level stack

→
- Longer wire length
- Looping sway control
- Thermal control

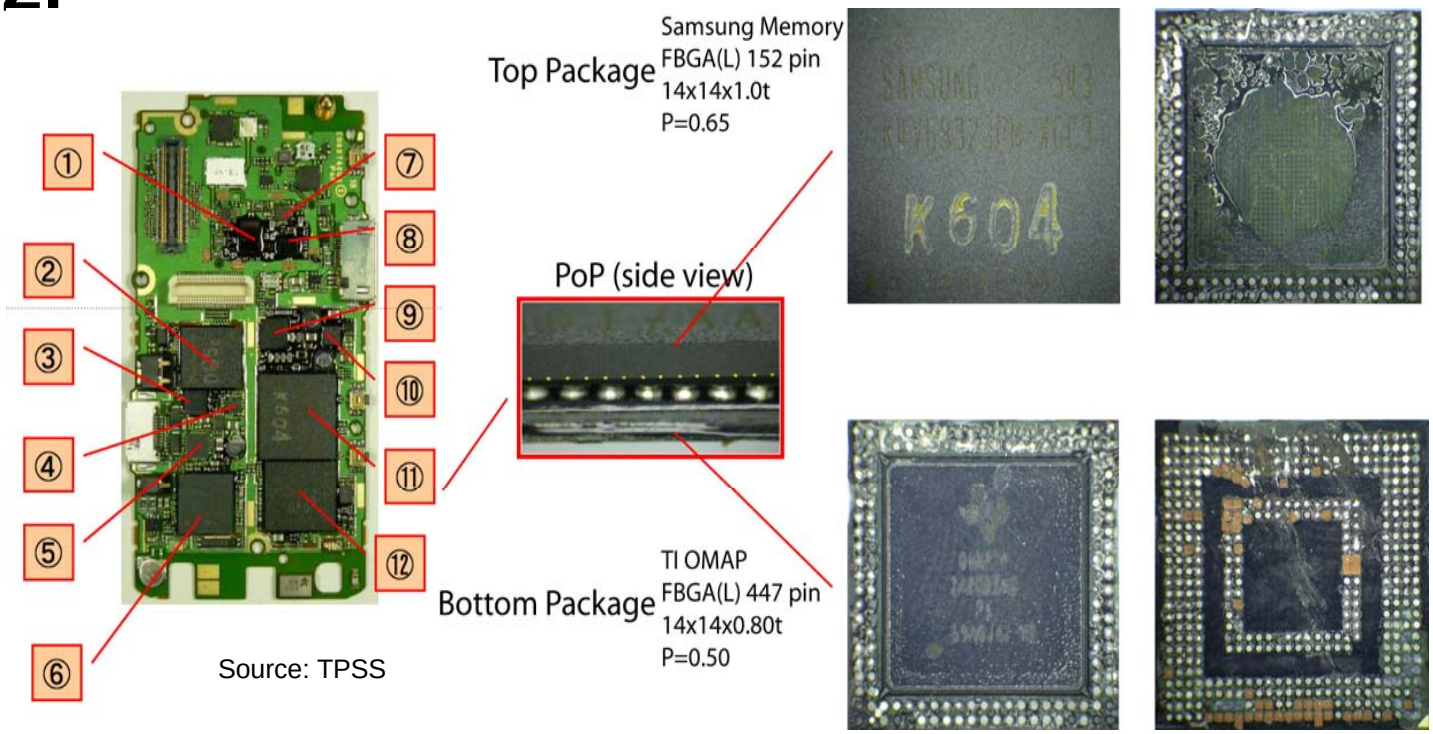
- Multi-function chips
  - From flash and SRAM to including ASIC and logic

→
- Finer pitch

Stacked Die Challenges

- Wafer thinning/die attach
  - Thickness of 75 µm in volume production today
  - Development work with thicknesses of 50 µm in development for both 8-inch and 12-inch wafers
  - Mechanical issues with dicing (handling, chipping, flaking)
- Wire bonding
  - Low loop heights, reverse bonding
  - Smaller diameter wire, longer spans
  - Die to die wire bonding can be complex
  - Die overhang (spacers required for same size die)
- Material selection
  - Substrates need to be thin, but rigid
  - Mold compound selection
- Thermal performance
- Business issues if logic + memory
  - Logistics
  - Testing (KGD)
  - Yield

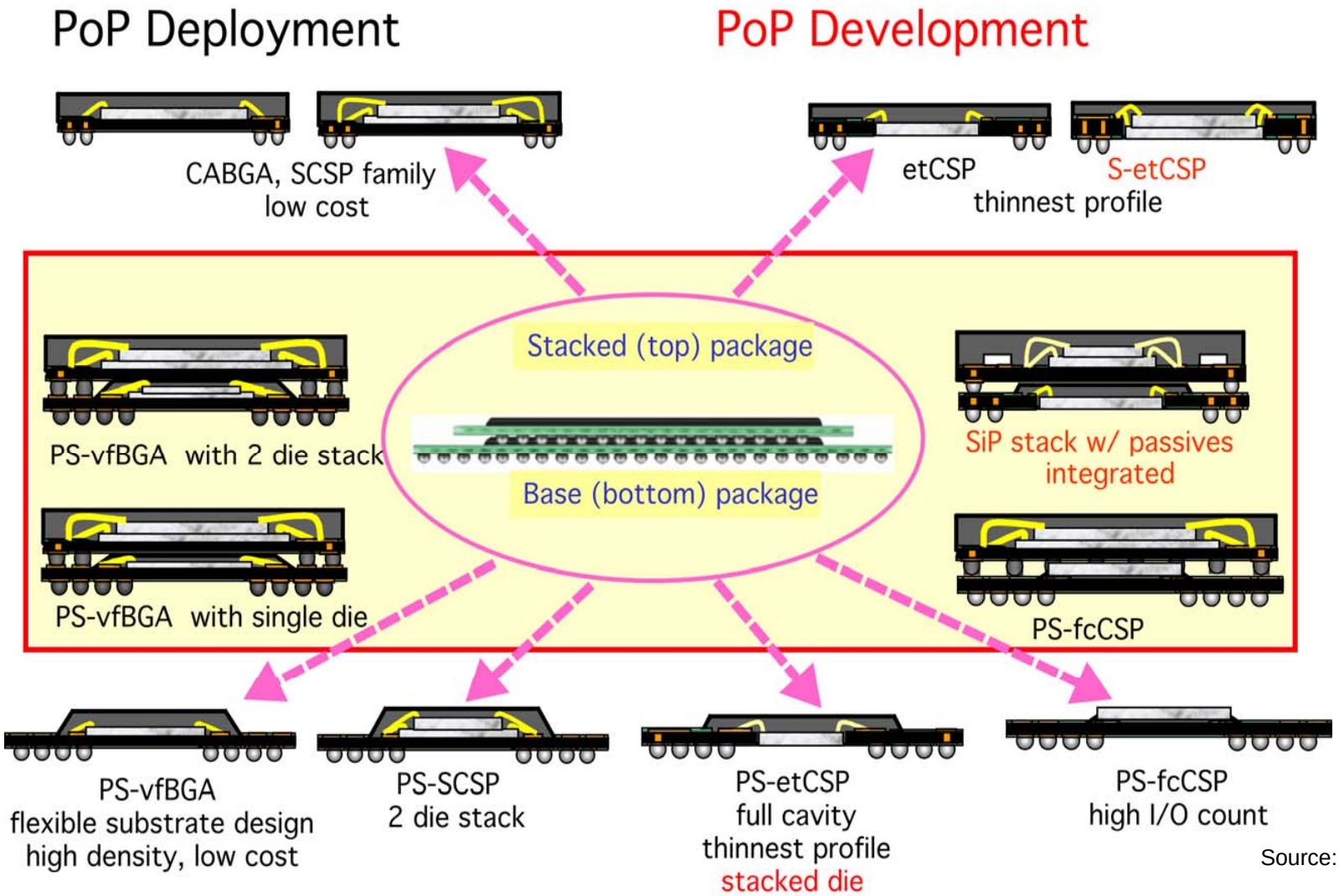
Package on Package (PoP) in Panasonic's P902i



- Individual packages stacked on top of each other, typically during board level assembly
- At least 10 major OEMs in handset and digital still camera market adoption PoP
- TechSearch estimates 67 million PoPs were shipped in 2006

Kulicke & Soffa

Amkor's PoP Options

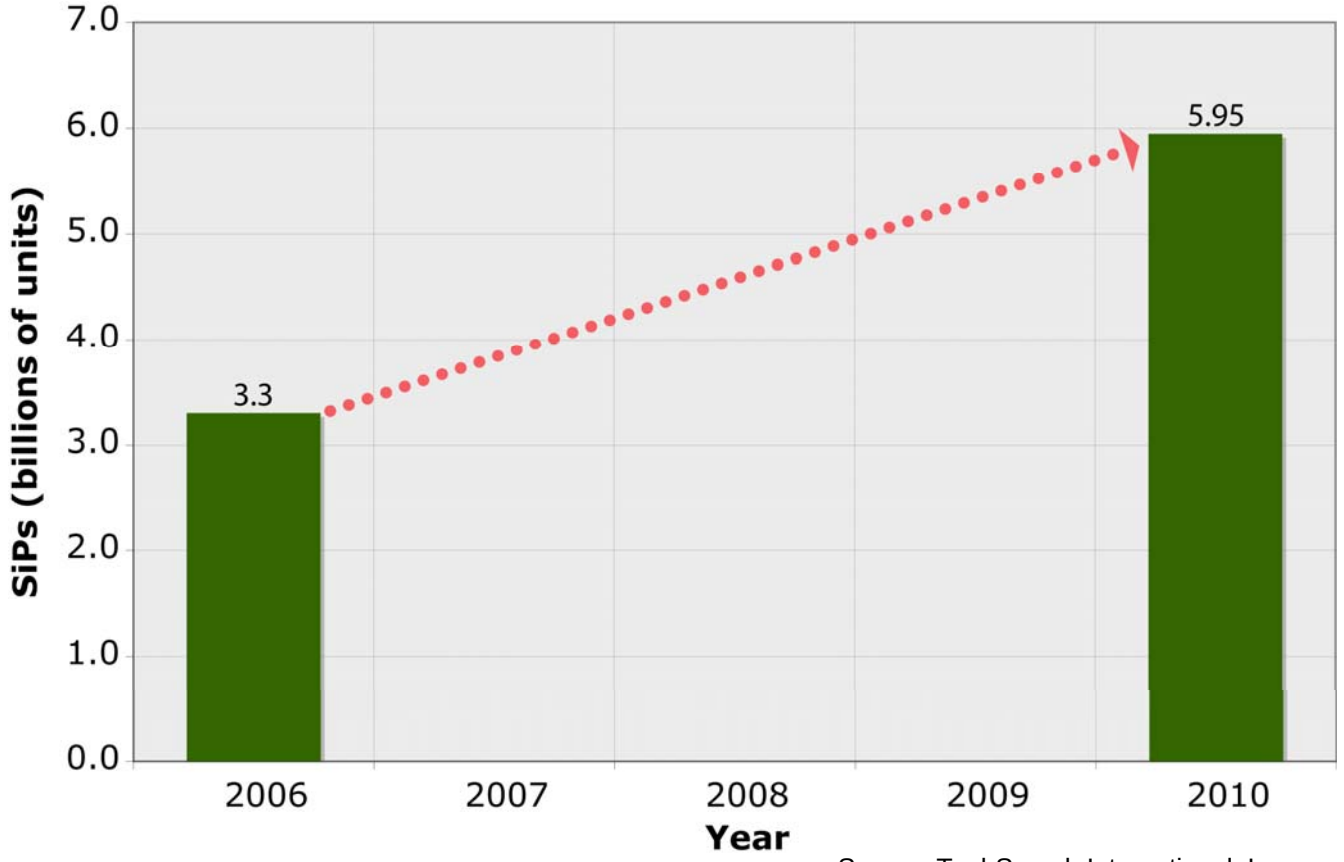


Source: Amkor

Kulicke & Soffa

SiP Growth

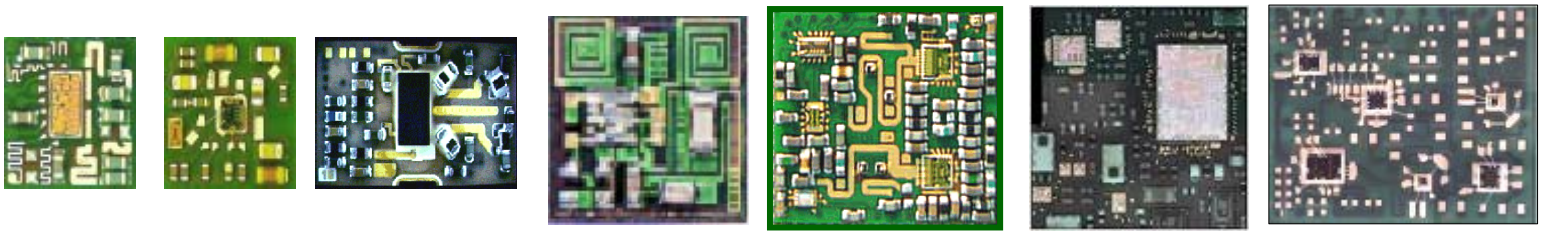
- Cell phones
- PDAs
- MP3 players
- Cameras
- Computers
- Automotive
- Medical
- Industrial
- Defense
- Aerospace



Source: TechSearch International, Inc.

- SiP is a functional system or subsystem assembled into a single package
- Utilizes combination of advanced packaging such as bare die (wire bond or flip chip), CSP, stacked package, stacked die
- CAGR of 15.9%

ASE Examples of SiP for Mobile RF

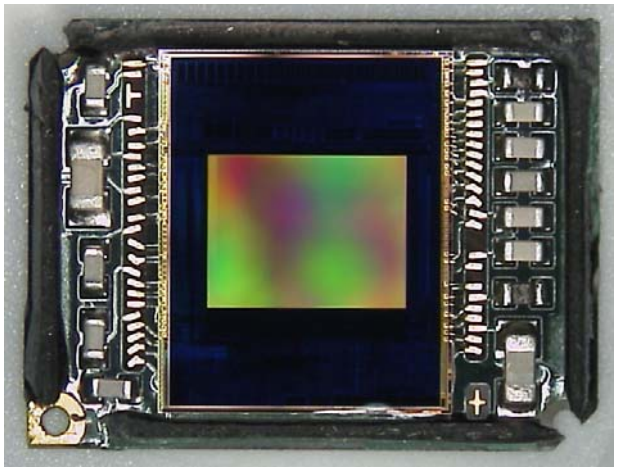


Source: ASE

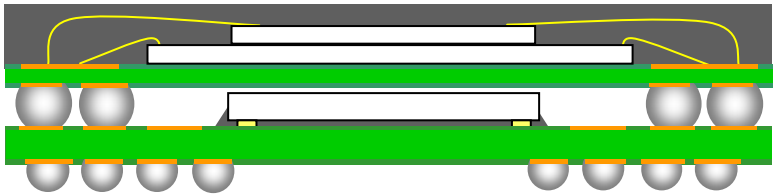
- Examples of PA (with antenna and switch), Transceiver, Front-End Module, DCR, SPR, BT, WLAN
- Module package size ranges from 3mm x 3mm to 13mm x 13mm
- Package thickness from 0.85 to 1.8 mm
- Die including silicon (min. 75µm thick), SiGe, GaAs HBT, pHEPT, CMOS, SAW/BAW filter
- Fine pitch wire bond 45 µm bond pad pitch

Note: DCR (Direct Conversion Receiver), SPR (Single Package radio), pHEMT (Pseudo-morphic High Electron Mobility Transistor), HBT (Hetero-junction Bipolar Transistor), CMOS (Complementary meta-Oxide Semiconductor)

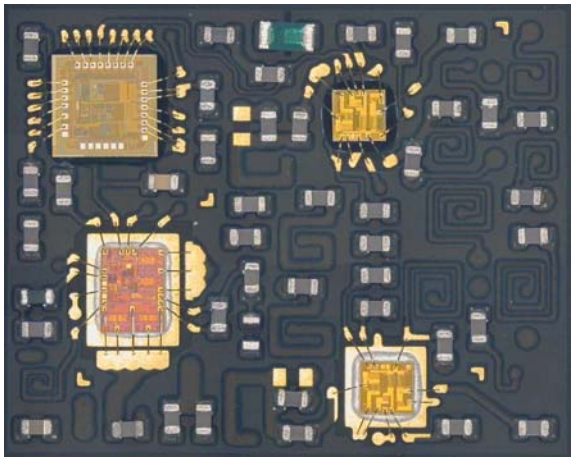
SiP Configurations in Mobile Phones



Source: TPSS



Source: Amkor

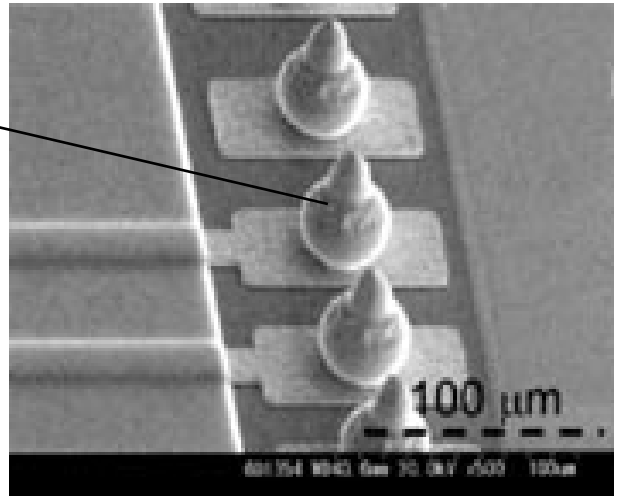


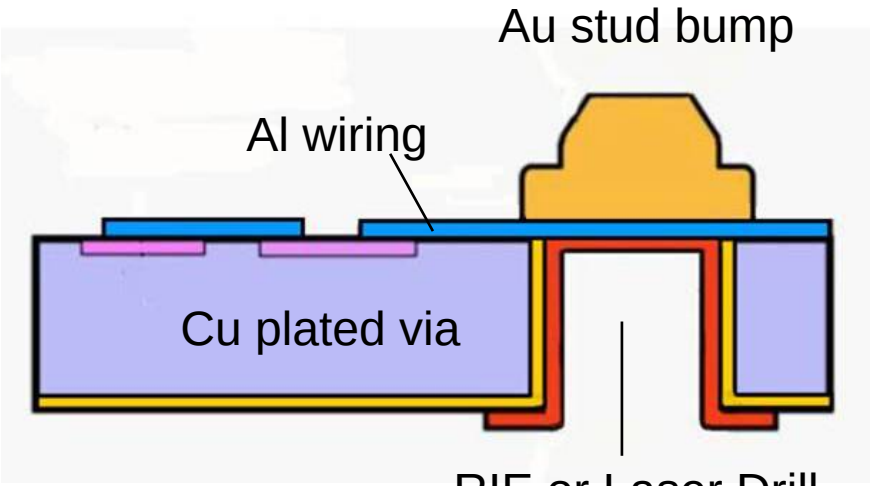
Source: Skyworks

- RF section
- Baseband section
- Camera module
- PA module

Future 3D TSV Camera Modules with Gold Stud Bump

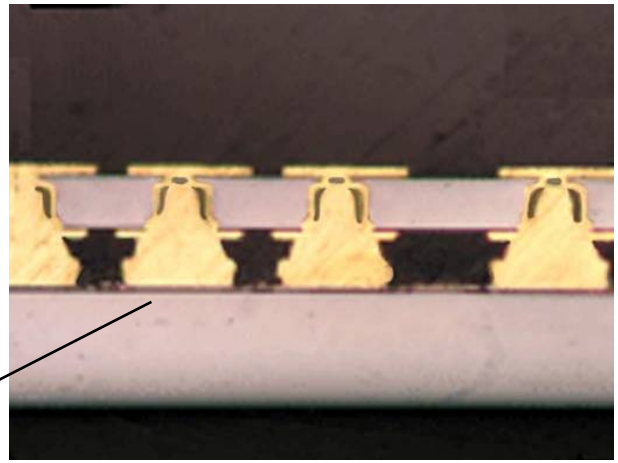
Stud bump made of Au wire



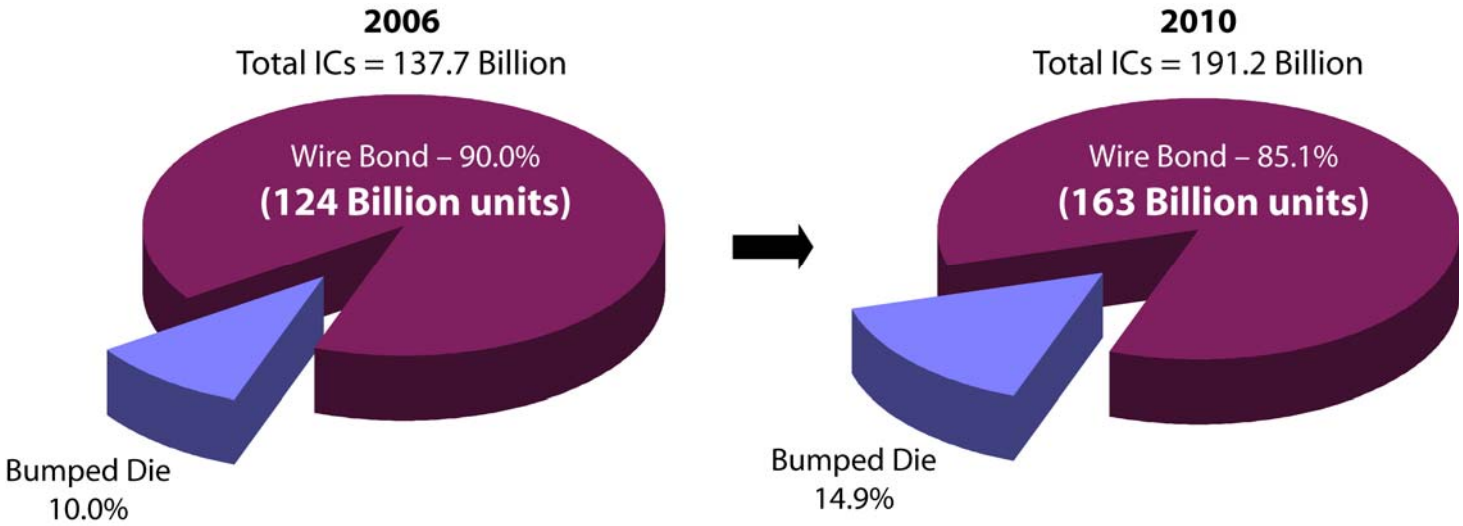


Source: Hitachi

Stacking cross section



Wire Bonding Market Share for IC Packaging

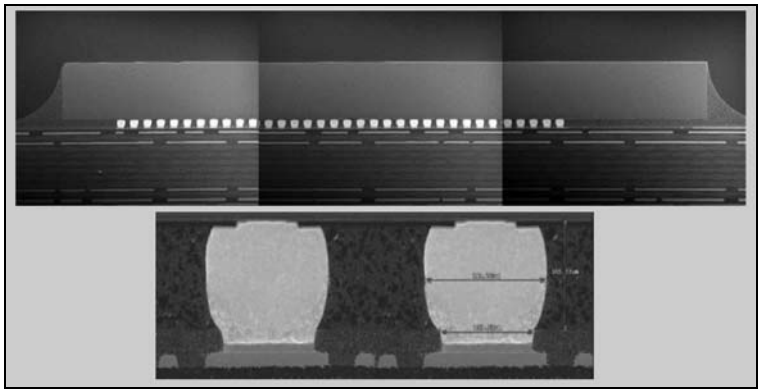


Source: IC Inisghts and TechSearch International, Inc.

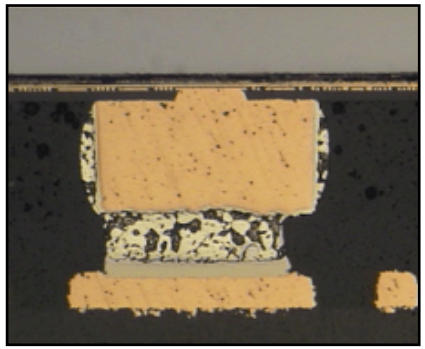
- Wire bonding remains the “mainstay” of the industry
- Bumped die includes flip chip, wafer level packages, gold bump driver ICs

Why Doesn't Flip Chip Dominate the Interconnect World?

- Flip Chip is used where needed, for performance or pad limited designs mostly, but in some cases form factor
  - Continued advances in wire bond technology
- Flip chip substrates are typically more expensive than wire bond substrates
  - Wire bond designs typically routed in four layers
  - Flip chip substrates are more complex, route bumped die with fine pitch
  - Flip chip often requires build-up substrates with lower yield, more expensive material sets, greater complexity



Source: ASE

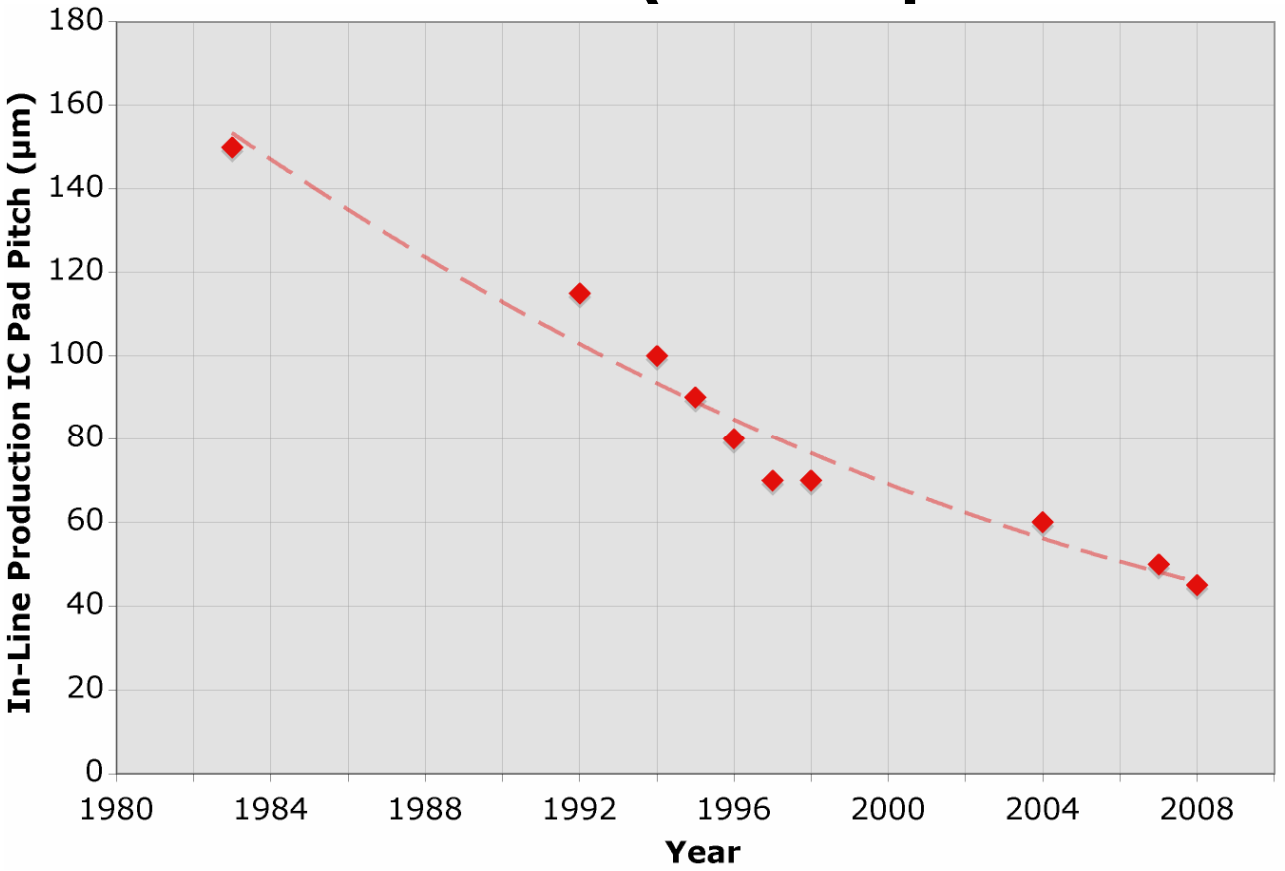


Source: ChipWorks

Why Doesn't Flip Chip Dominate the Interconnect World?

- Many companies have found that flip chip assembly is typically more expensive than wire bond
  - Flip chip substrate shortage in 2005 increased substrate prices, with current overcapacity substrate prices are falling again
  - Intel has twice delayed the move from wire bond to flip chip for the ICH chipset (Southbridge), current delay shifts flip chip adoption out to 2009
  - Estimated assembly cost for wire bond vs. flip chip in large die size 17mm x 17mm found flip chip assembly was 30% more expensive than wire bond (even without consideration of substrates)

Wire Bond Pitch Trends (actual production)

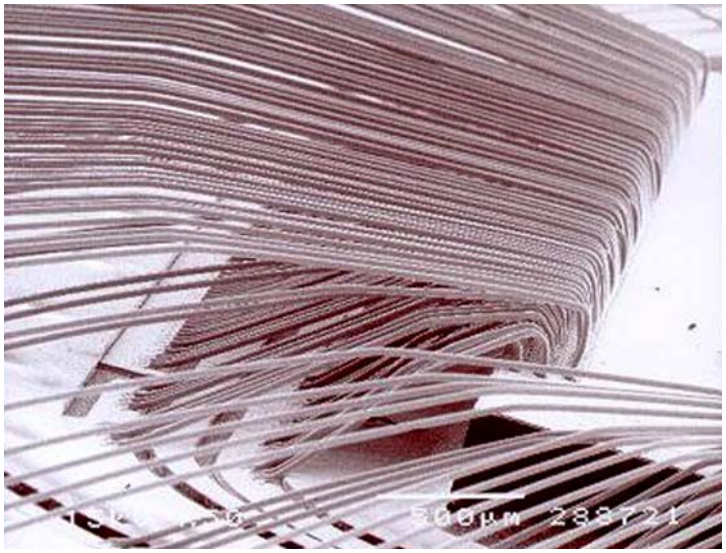


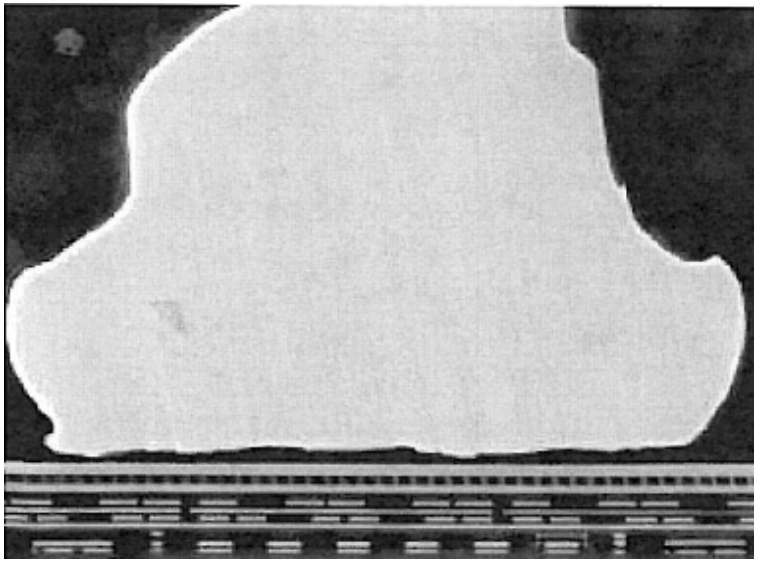
Source: TechSearch International, Inc.

- Wire bond pitch in actual production has become finer and finer over time, trend continues

Bond Pad Over Active I/O

- LSI developed the industry's first wire bond over active I/O technology (Pad on I/O™) for copper/low-k
- Allows the extension of wire bond technology to deep submicron CMOS designs in 130nm and 90nm nodes that are typically pad limited
- Placing wire bonds over the active I/O saves die area and does not affect metal routing and interconnect
- Can be used for in-line or staggered pad designs (27µm effective)





Source: LSI

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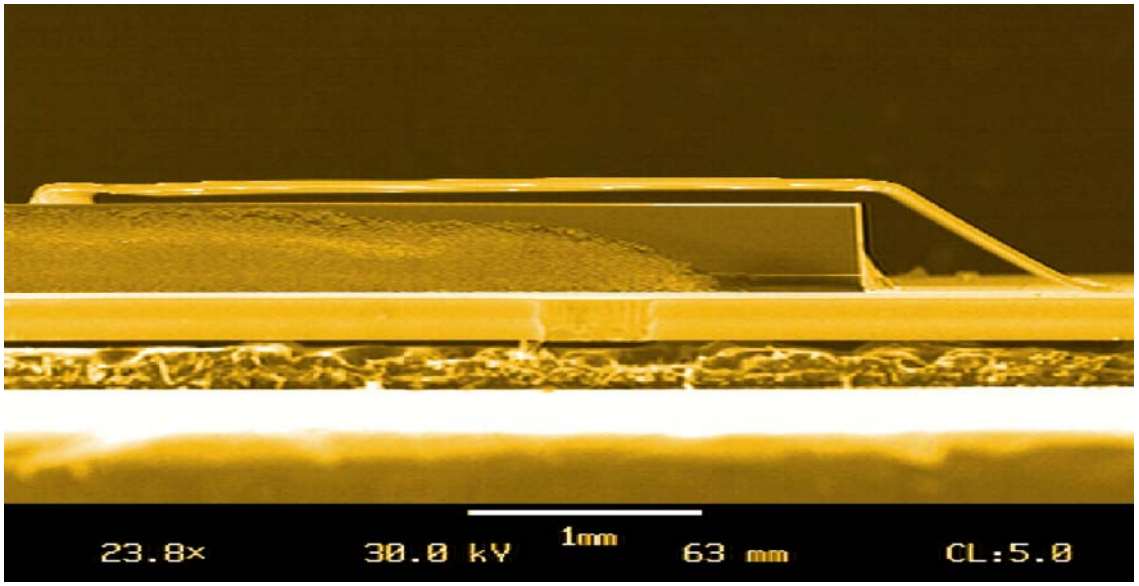
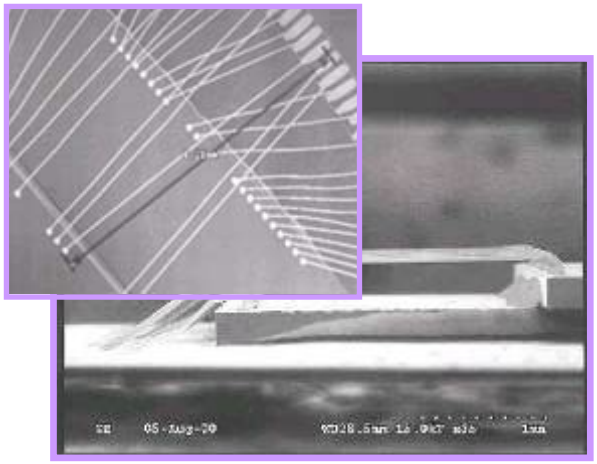
New Developments in Low Loop Height Wire Bonding

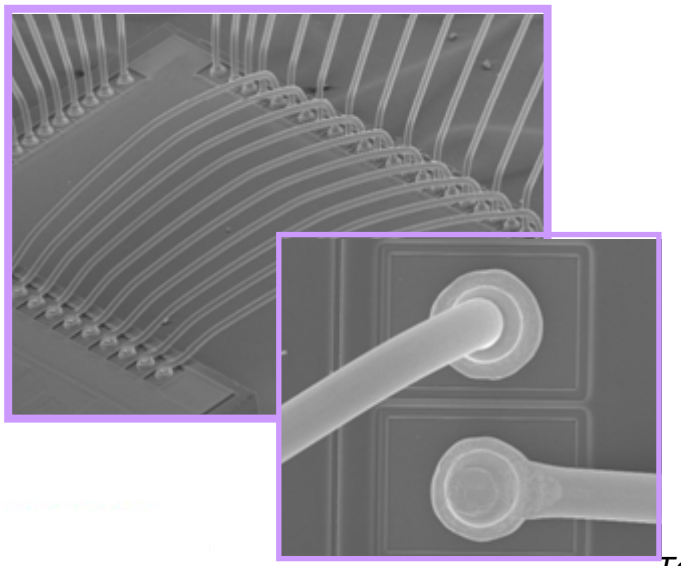


Source: K&S

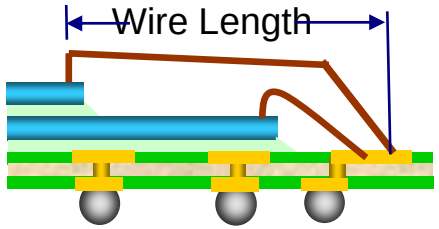
- Specially designed for stacked die applications
- Highly accurate and consistent loop profiles
- Improved loop linearity and stability
- Higher bond test results

ASE's Wire Bonding Capability





- **Long length capability**

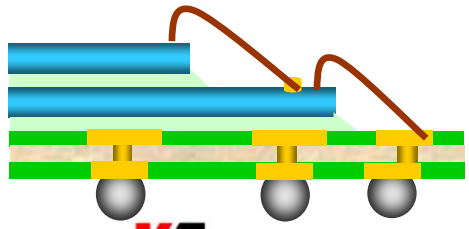


Max. Wire Length (MWL)	Wire Diameter	Bond Pad Opening
3.8mm(150mil)＜ MWL ≦ 4mm(160mil)	30um(1.2mil)	B.P.O.≧80(um)
3.5mm(140mil) ＜ MWL ≦ 3.8mm(150mil)	28um(1.1mil)	B.P.O.≧63(um)
3.3mm(130mil)＜ MWL ≦ 3.5mm(140mil)	25um(1.0mil)	B.P.O.≧53(um)
3mm(120mil) ＜ MWL ≦ 3.3mm(130mil)	23um(0.9mil)	B.P.O.≧43(um)
MWL ≦3mm(120mil)	20um(0.8mil)	B.P.O.≧40(um)

- **Die to Die Bonding**

  65 µm bonding pad pitch Min.

  55 µm bond pad open Min.



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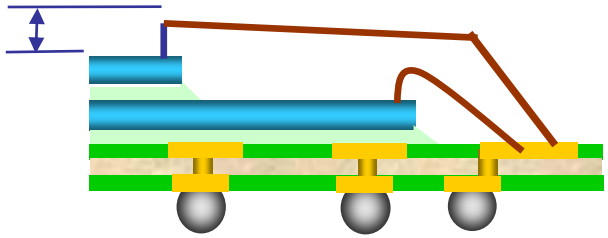
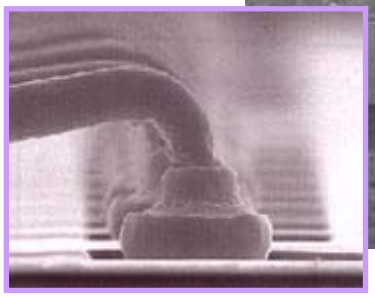
ASE's Wire Bonding Capability

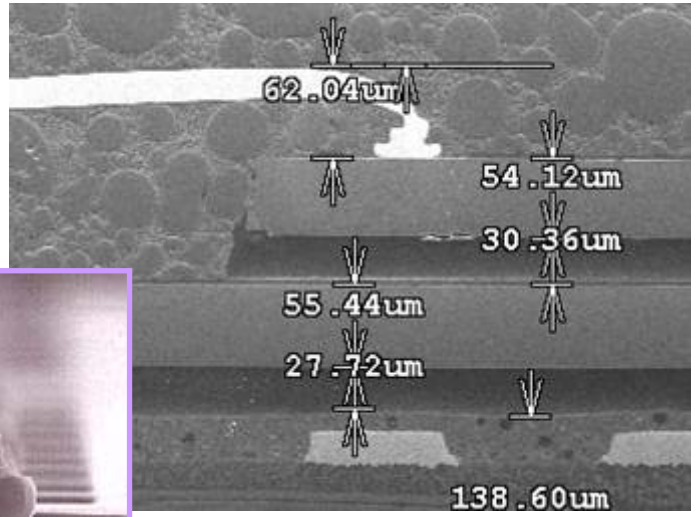
✓ Forward bond-standard

Min. loop height : 75µm (20µm wire)

Loop Height



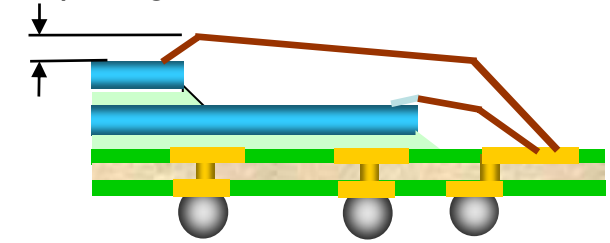


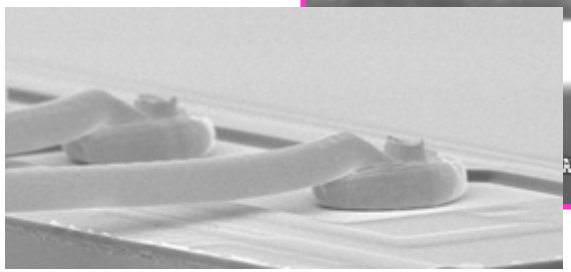


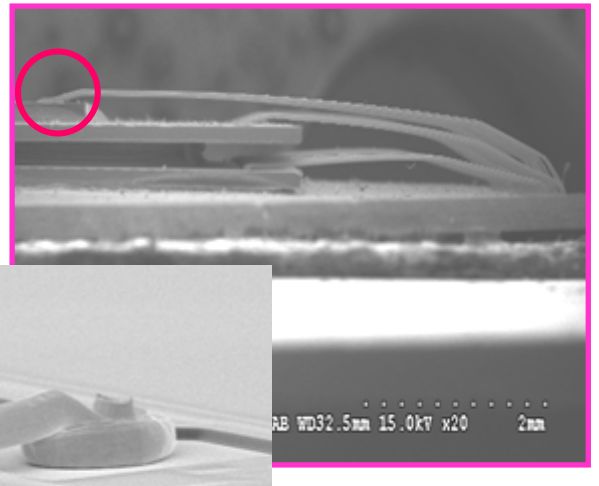
✓ Reverse bond

Min. loop height : 50µm (20µm wire)

Loop Height







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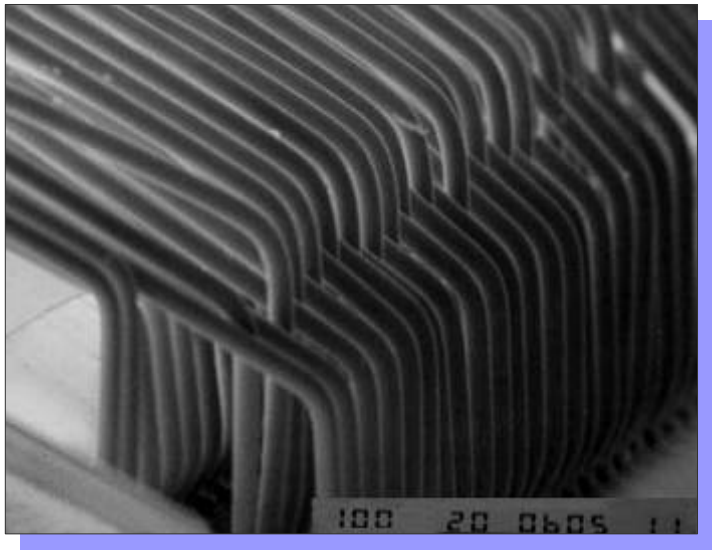
Microbonds X-Wire™ Technology

- X-Wire™is a coated wire bond technology
  - Proprietary process developed to coat wire
- X-Wire™ allows greater design flexibility:
  - Relax tight wire bonding rules and corner pad rules
  - Relax loop profiling and wire connection violations
  - Allows crossing, touching wires and long wires

Bare Wire



X-Wire™

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Conclusions

- Advanced packaging continues to grow in units and revenue
  - IC package subcontractors improve revenue growth with advanced package assembly
- Advanced packaging ≠ FC
- Wire bond accounts for 90% of IC packages shipped in 2006
- Advanced packaging includes BGAs, CSPs, flip chip, and wafer level packages
  - Wire bond accounts for 67% of all advanced packages
  - Strong unit volume growth in a variety of packages including stacked die, SiP, BGA, and all types of CSPs

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